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# Simulation of Carrier Mobility in Silicon Gate-All-Around (GAA) Nanotransistors

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**Abstract.** We studied the impact of scattering mechanisms on carrier mobility in the active region of ultrathin silicon gate-all-around (GAA) cylindrical nanotransistors. Using numerical simulation tools and carrier scattering models, we analyzed how these mechanisms affect carrier mobility. We applied statistical methods to estimate mobility variation across 3 to 8 nm channel diameters and 200 to 400 K temperatures.

**Keywords**: silicon gate-all-around (GAA) nanotransistor, carrier mobility, temperature variation, simulation

## 1. Introduction

To unleash the industrial capabilities of ultrathin silicon gate-all-around nanotransistors, we need dependable analysis techniques and a deep understanding of the device physics. One approach we implemented in our earlier research is a combination of a quantum method (the Schrödinger equation) and a semi-classical Boltzmann transport equation. In this way, we consider the key scattering mechanisms, such as phonon scattering, surface roughness, scattering at ionized impurities, and traps at the silicon-silicon oxide interface. This comprehensive approach is beneficial to the simulation of advanced, technologically relevant nanostructures that can be manufactured today [1].

The GAA concept enhances charge control in the nanotransistor's active region, minimizes short-channel effects (SCE), and improves transport properties. It also offers advanced materials and technologies to boost chip performance. Another benefit of ultrathin silicon gate-all-around nanowire transistors is that they can be scaled down to 5 nm [2–5]. For GAA simulation and optimization, methods that integrate quantum-mechanical effects (QME) into semi-classical transport frameworks [6-8] are particularly appealing as they are less computationally intensive than pure quantum transport and atomistic approaches [9–11]. The self-consistent semi-classical method is still important for dependable simulation of the electronic transport characteristics in devices smaller than 10 nm [8].

In this study, we combined numerical simulation tools and carrier scattering mechanism models to simulate the transport properties of ultrathin silicon gate-all-around (GAA) cylindrical nanotransistors. The objective is to investigate the physical effects that influence carrier mobility in the operating region of these nanodevices. The focus on mobility stems from its electrical nature related to how efficiently carriers move through the transistor.

## 2. Materials and Methods

In low-dimensional systems, charge carriers (such as electrons or holes) cannot be considered point particles. Therefore, in a direction perpendicular to the transistor's axial axis, the momentum of a localized carrier is not precisely defined due to the uncertainty principle. Consequently, the carrier's energy is quantized within an individual subband. In this scenario, the characteristics of each scattering process depend on the extent to which the carrier eigenfunctions overlap within each such subband [12].

The electron mobility in thin silicon gate-all-around (GAA) nanotransistors can be determined using a quasi-analytical method applied to each zone. In this case, the mechanisms of electron scattering by (acoustic and optical) phonons, charged impurities, roughness, and traps at the $Si\text{-}SiO_2$ interface, which limit carrier mobility in the transistor channel, are considered independently. In this scenario, for the i-th scattering mechanism and the k-th subband, the mobility is expressed as:

$$\mu_{i,k} = \frac{2q\beta}{N_k m_k} \int \tau_{i,k}(E) g_k(E)(E - E_k) f_o(E) \times \times (1 - f_o(E)) dE$$

where $q$ is the elementary charge; $\beta=(k_B T)^{-1}$, $k_B$ is the Boltzmann constant; $T$ is the temperature; $m_k$ is the effective carrier mass in the k-th subband; $\tau_{i,k}$ is the relaxation time, $g_k$ is the one-dimensional density of states, $f_0$ is the Fermi-Dirac function; and $N_k$ is the one-dimensional electron concentration in the k-th subband, given by the equation

$$N_k = N_{eff}\left[-\Im\{\frac{1}{2}, -\exp(\beta(E_F - E_k))\right],$$

where $N_{eff}$ is the effective one-dimensional density of states, $\Im$ is the Fermi integral of order 1/2, and $E_F$ is the Fermi level. Since multiple scattering mechanisms are combined, the total mobility for each subband should account for their cumulative effect, as determined by the well-known Matthiessen's rule.

Alternatively, to study the variations in charge mobility, their transport is analyzed using a semi-classical approach by solving the Boltzmann transport equation (BTE). The BTE solution relies on the approximation of the relaxation time, which essentially linearizes the equation. Our calculations used the approximation of ellipsoidal non-parabolic valleys with a zonal structure; while transitions between the two states occur instantaneously, as we implemented in our earlier studies.

## 3. Results and Discussion

The GAA nanotransistor's structure is shown in Figure 1. It features a cylindrical silicon nanowire with a [100] channel orientation, encased in a thin silicon dioxide layer with a 1 nm equivalent oxide thickness, and includes thickened drain and source regions. Initially, the transistor channel diameter is 5 nm. The nanotransistor incorporates spacers (gaps) between the highly doped drain and source regions and the undoped channel. The spacer length is fixed at 5 nm, and its diameter matches that of the active region.

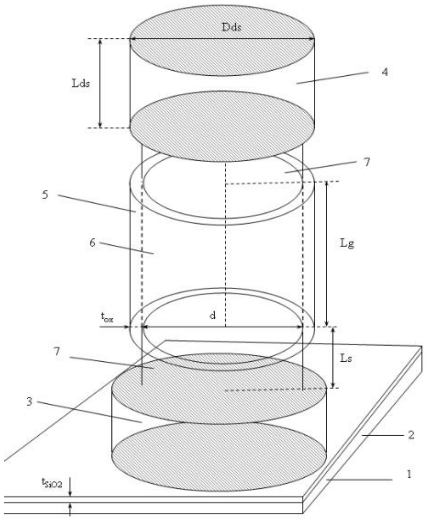


Figure 1. Silicon cylindrical gate-all-around (GAA) nanotransistor, where 1 is the silicon substrate, 2 is the silicon oxide film, 3 is the source, 4 is the drain, 5 is the gate insulator, 6 is the active region, Lds is the drain/source length, Dds is the drain/source diameter, d is the active region diameter, Lg is the active region length, Ls is the spacer length.

Such a design streamlines the device manufacturing by eliminating the need to create sharp boundaries between the drain/source and the active region (AR). However, it does not decrease the probability of impurity diffusion from the heavily doped areas into the AR. In this case, we need to further investigate the effect of charged impurities on the GAA nanotransistor performance. All prototype drain and source regions featured identical doping profiles, with a peak Nds at $1\times10^{20}$ cm$^{-3}$ at the outer edge of these regions. For the simulation, we randomized only arsenic atoms using the Monte Carlo kinetic method [13, 14]. They are distributed as point potentials within the channel. We considered both long-range and short-range Coulomb potentials. Our analysis covered a wide range of equivalent ionized impurity (dopant) concentrations, with Ndi ranging from very low ($10^{15}$ cm$^{-3}$) to high ($10^{18}$ cm$^{-3}$). The density of states at the Si-$SiO_2$ interface varies from $10^{11}$…$10^{13}$ cm$^{2}$. The AR surface is defined parametrically, with a 5 nm correlation length and an RMS ranging from 0.2 to 0.5 nm. We assessed the mobility at a drain supply voltage (Uds) is equal 0.05 V and a gate supply voltage (Ugs) is equal 0.8 V.

Figure 2 shows the electron mobility curve $\mu(N_{di})$ when limited solely by ionized impurity.

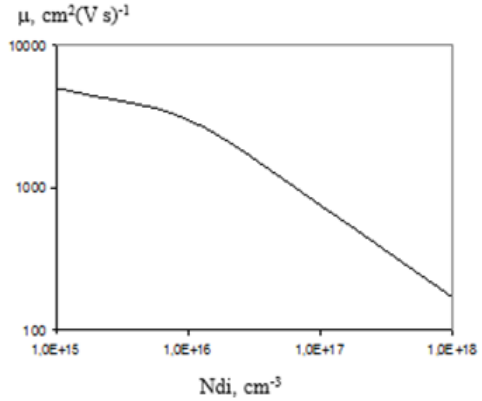


Figure 2. Carrier mobility curve when limited solely by the ionized impurity level in the channel

At high $N_{di}$ levels exceeding 3x$10^{16}$ cm$^{-3}$, since the scattering rate from at a charged impurity is directly proportional to its density, the mobility decreases as $\mu \sim 1/N_{di}$. A sharp decline in mobility as the $N_{di}$ level rises indicates that this mechanism is a dominant contributor at high concentrations.

Figure 3 shows the carrier mobility vs. density of traps ($N_f$) at the silicon–silicon oxide interface, considering the effects of scattering by acoustic and optical phonons, while excluding contributions from surface roughness and ionized impurities.

Note that phonon-induced mobility degradation is essentially constant and independent of external factors.

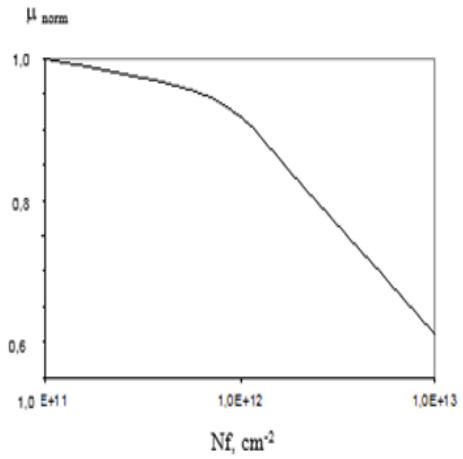


Figure 3. carrier mobility vs. density of traps at the Si-$SiO_2$ interface

At the highest carrier density, the mobility limited by phonon-electron interactions is 200 $cm^2/V \cdot s$. The scattering rate from acoustic phonons is higher than that from optical phonons, so the effect of the former mechanism on mobility is much more significant. As in the previous case, mobility decreases monotonically, but the effect is smaller. This behavior occurs under a strong perpendicular component of the electric field.

Figure 4 shows the AR mobility vs. the cross-sectional diameter, considering all scattering mechanisms under the worst-case conditions for impurities, traps, and the RMS surface roughness.

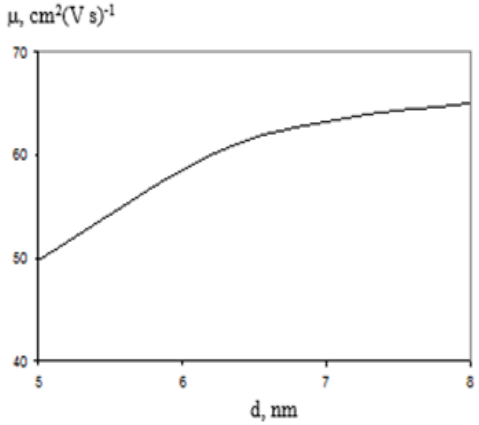


Figure 4. Electron mobility vs. the diameter, considering the combined effects of scattering

The impact of surface roughness scattering is minimal at low carrier densities. The intensity becomes significant at a $3.25 \times 10^{12}$ $cm^{-2}$ carrier density. This mechanism is becoming the dominant one. In this scenario, the carrier density is directly regulated by adjusting the gate voltage Ugs. As the gate voltage rises, the density also increases. All our conclusions remain valid for every subband within the three relevant conduction valleys, considering that most electrons occupy the lowest subband. As the diameter increases, the mobility improves due to a reduced impact of the impurity injected from the source/drain regions into the transistor channel. An even greater effect can be achieved by increasing the spacer's linear dimension.

Figure 5 shows how the parameter Δ affects mobility across the entire Ndi range at the highest trap level.

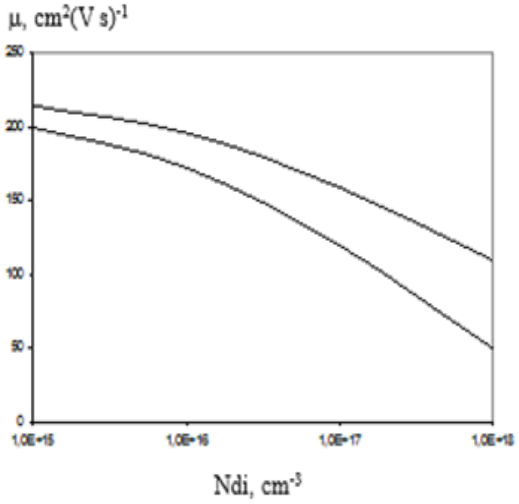


Figure 5. Mobility vs. the ionized impurity concentration at different Δ. Lower curve: Δ= 0.5 nm; upper curve: Δ= 0.2 nm

These findings demonstrate the substantial adverse impact of the injected impurity on carrier mobility. In the worst-case scenario, the difference exceeds 30%. Therefore, there is a need to develop technologies to prevent impurity diffusion from the drain/source regions, while also reducing the roughness of the Si-$SiO_2$ interface. It is a critical challenge for both ultrathin GAAs and FinFET transistors.

A key benefit of silicon GAA nanotransistors is their operation at low AR doping levels, resulting in minimal statistical variability in their electrophysical properties [15]. Note that various mechanisms contribute to the spread of mobility. Surface roughness is the primary factor restricting mobility and causing its high variability. Its sole advantage is its temperature invariance, meaning the carrier scattering rate is not affected by temperature. Therefore, the mobility variations with temperature are affected only by scattering at impurities and traps. However, minimizing the field components perpendicular to the direction of transport can help reduce the impact of these parameters on the variability of the transistor's electrophysical properties.

Figure 6 illustrates the mobility variations $\sigma\mu$ (see above) vs. AR diameter.

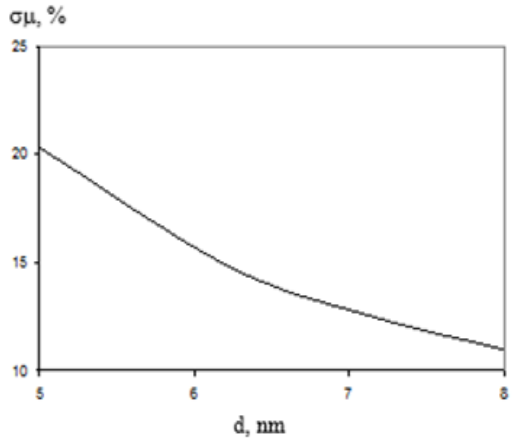


Figure 6. σμ(d) curve

The magnitude of mobility variations increases with the diameter d. The change in the standard deviation across the considered range of d is approximately 50%. This value can also be decreased by enlarging the spacer's linear dimensions. Relative mobility variations define a trend characteristic of the relative fluctuations in the drain-source current Ids. Note that their ranges are approximately equal when expressed as percentages.

Figure 7 illustrates the temperature curve $\sigma\mu(d)$ in the 200–400 K range, assuming the transistor operates normally within this temperature range.

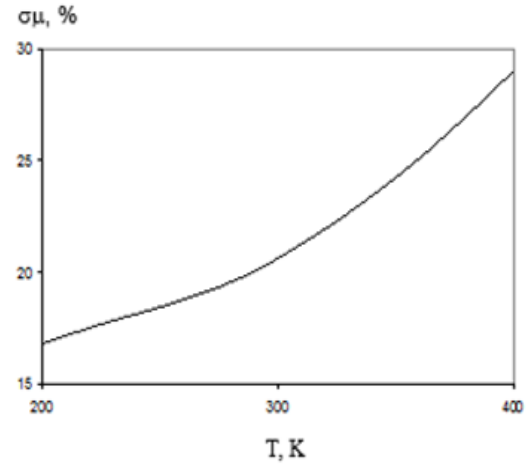


Figure 7. $\sigma\mu(T)$ curve

Also note that the $\sigma\mu(T)$ curve closely follows a $\sigma\mu(T) \sim T^{\Upsilon}$ parabolic curve where $\Upsilon$ = 0.69. The $\Upsilon$ coefficient depends on the AR topology. Figure 8 shows, in normalized coordinates relative to the curve presented in Figure 7, the $\sigma\mu_{norm}(T_{norm})$ curves for various AR diameters. In this instance, the 200–400 K temperature range is normalized to a 0 to 1 range. The normalized parameter $\sigma\mu$ is derived by dividing by $\sigma\mu$ $(T = 400K)$ for d = 5 nm.

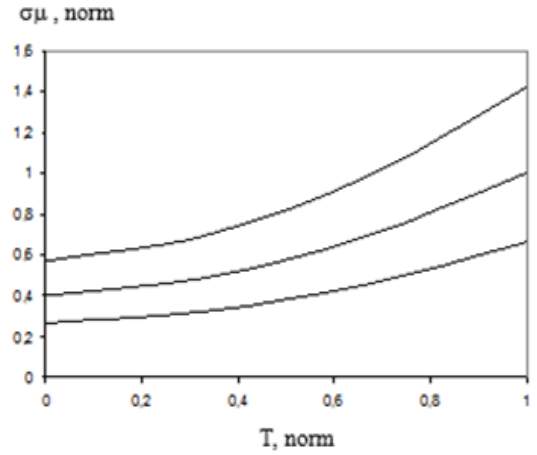


Figure 8. Normalized curve $\sigma\mu_{norm}(T_{norm})$ for various diameters. Upper curve: d=3 nm; middle curve: d=5 nm; lower curve: d=8 nm.

Note that the function's $\sigma\mu(T)$ nature remains unchanged, but the coefficient $\Upsilon$ differs for each diameter. However, it does not exceed 1.

A lower gate voltage will decrease $\sigma\mu(T)$. A 0.1 V change in Ugs results in a 3% to 9% reduction in $\sigma\mu(T)$ depending on the transistor's AR topology and ambient temperature.

## 5. Conclusion

Using numerical simulation tools and models of carrier scattering mechanisms, we numerically studied how these mechanisms combined affect carrier mobility in ultrathin silicon gate-all-around cylindrical transistors. The application of this analysis is to demonstrate how different mechanisms affect carrier mobility. and provide estimates of the potential impact on device performance. We applied statistical methods to estimate mobility variation across 3 to 8 nm channel diameters and 200 to 400 K temperatures.

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